What is claimed is:

1. A converter device having an A/D converter unit for converting AC power to DC power and a power factor improving unit for improving a power factor of said A/D converter unit,

wherein said power factor improving unit comprises,

a photocoupler for converting an AC power-supply waveform given to said A/D converter unit into a digital signal and outputting said digital signal,

a computer system for generating full-wave rectification waveform data synchronized with said AC power-supply waveform on the basis of said digital signal,

a D/A converter receiving as a reference voltage a voltage error signal based on a voltage error between a predetermined set voltage and an output voltage of said A/D converter unit, for multiplying together said reference voltage and said full-wave rectification waveform data to output a target current value waveform similar to the waveform of an input voltage in said A/D converter unit, and

a current control portion for comparing said target current value waveform and a waveform of a current flowing in said A/D converter unit and controlling said current flowing in said A/D converter unit to reduce a current error between the two.

2. The converter device according to claim 1,

wherein a voltage error signal generating portion for generating said voltage error signal and said current control portion are provided inside an IC chip as a power factor improving circuit, and

said D/A converter and said computer system are provided outside said IC chip.

3. The converter device according to claim 2, wherein said D/A converter is provided inside said computer system.

4. The converter device according to claim 2, wherein said D/A converter is provided outside said computer system.

5. The converter device according to claim 1, wherein said D/A converter, a voltage error signal generating portion for generating said voltage error signal, and said current control portion are provided inside an IC chip as a power factor improving circuit and said computer system is provided outside said IC chip.

6. The converter device according to claim 1, wherein said D/A converter, said computer system, a voltage error signal generating portion for generating said voltage error signal, and said current control portion are provided inside an IC chip as a power factor improving circuit.

7. The converter device according to claim 6,

wherein said computer system comprises:

a storage device in which source data about a full-wave rectification waveform for one period of said AC power-supply waveform is written as digital data; and

an address generating circuit receiving said digital signal outputted from said photocoupler, for outputting an address signal with a given timing and thereby adjusting time intervals at which said digital data written in said storage device is inputted to said D/A converter,

and wherein said address generating circuit adjusts said time intervals to

establish synchronization with a cycle of said AC power-supply waveform, and

said storage device outputs said full-wave rectification waveform source data in correspondence with said address signal given from said address generating circuit so as to provide to said D/A converter said full-wave rectification waveform data synchronized with said AC power-supply waveform.

8. The converter device according to claim 7, wherein said power factor improving circuit contains in said IC chip an oscillation circuit for giving a reference clock signal to said address generating circuit.

9. The converter device according to claim 8, wherein said oscillation circuit has a variable resistor and a variable capacitor as a resistance component and a capacitance component determining its oscillation frequency.

10. The converter device according to claim 8, wherein said oscillation circuit has, outside said IC chip, a resistance component and a capacitance component determining its oscillation frequency.

11. The converter device according to claim 8,

wherein said oscillation circuit is a voltage-controlled oscillator circuit, and

said power factor improving circuit further contains, inside said IC chip, a PLL circuit for locking an output of said voltage-controlled oscillator circuit and giving the output to said address generating circuit.

12. The converter device according to claim 8,

wherein said address generating circuit comprises:

a frequency-dividing circuit for frequency-dividing said reference clock signal; and

an address counter for counting said reference clock signal converted to a lower frequency by said frequency-dividing circuit to determine the timing of output of said address signal.

13. The converter device according to claim 7, wherein said power factor improving circuit obtains, from outside of said IC chip, a reference clock signal to be given to said address generating circuit.

14. The converter device according to claim 13, wherein said address generating circuit comprises:

a frequency-dividing circuit for frequency-dividing said reference clock signal; and

an address counter for counting said reference clock signal converted to a lower frequency by said frequency-dividing circuit to determine the timing of output of said address signal.

15. The converter device according to claim 7,

wherein said address generating circuit comprises:

a frequency-dividing circuit for frequency-dividing said reference clock signal;

a period counter receiving said digital signal outputted from said photocoupler, for counting a count value for one period of said AC power supply on the basis of said reference clock signal converted to a lower frequency by said frequency-dividing circuit;

division means for dividing said count value by the number of data of said full-wave rectification waveform source data to obtain a divided value corresponding to a period of increment of an address in said storage device;

a register for storing said divided value;

a timer counter for counting said divided value on the basis of said reference clock signal converted to the lower frequency by said frequency-dividing circuit; and

an address counter for determining the timing of output of said address signal on the basis of said divided value.

16. The converter device according to claim 15, wherein said division means is a division circuit.

17. The converter device according to claim 15, wherein said division means is a storage device for storing results of division in which results of a predetermined division are previously written.

18. The converter device according to claim 15, wherein said division means includes said period counter and obtains said divided value by bit-shifting a result counted by said period counter.